-- FIGs. 1A and 1B, arranged as shown in FIG. 1, are a diagram of a typical digital network showing the interconnection of a network node to the network and the components of the network node according to the preferred embodiment of this invention.--

In the Claims

Please amend claims 1, 31-34, and 37-39, as follows:

1. [Twice Amended] A cache coherency system for a shared memory parallel processing system including a plurality of processing nodes, comprising:

a multi-stage communication network for interconnecting said processing nodes;

each said processing node including a unique section of shared memory which is not a cache;

each said processing node including one or more caches for storing a plurality of cache lines;

a cache coherency directory which is distributed to each of said nodes for tracking which of said nodes have copies of each cache line; and

an adapter for storing changed data immediately to said unique section of shared memory regardless of which of said nodes is changing the data and which of said nodes includes the section of shared memory to be changed, such that said shared memory always contains the most recent data.

31. [Amended] A method for operating a shared memory parallel processing system as a cache coherency system including a plurality of processing nodes, each said processing node including a unique section of shared memory which is not a cache, comprising the steps of:

interconnecting said processing nodes through a multi-stage communication network;

storing at each said processing node a plurality of cache lines in one or more caches;

distributing to each of said processing nodes a cache coherency directory;

tracking in said cache coherency directory which of said processing nodes have copies of each cache line; and

changing said shared memory, wherein changed data is stored immediately to said unique section of shared memory regardless of which of said nodes is changing the data and which of said nodes includes the section of shared memory to be changed, wherein said shared memory always contains the most recent data.

32. [Amended] A program storage device readable by a machine, tangibly embodying a program of instructions executable by a machine to perform method steps for operating a shared memory parallel processing system including a plurality of processing nodes, each said processing node including a unique section of shared memory which is not a cache, said method steps comprising:

interconnecting said processing nodes through a multi-stage communication network;

storing at each said processing node a plurality of cache lines in one or more caches;

tracking in a cache coherency directory which is distributed to each of said processing nodes which of said processing nodes have copies of each cache line; and

changing said unique section of shared memory, wherein changed data is stored immediately to shared memory regardless of which of said nodes is changing the data and which of said nodes includes the section of shared memory to be changed, wherein said shared memory always contains the most recent data.

33. [Amended] An article of manufacture comprising:

a computer useable medium having computer readable program code means embodied therein for operating a shared memory parallel processing system including a

plurality of processing nodes, each said processing node including a unique section of shared memory which is not a cache, the computer readable program means in said article of manufacture comprising:

computer readable program code means for causing a computer to effect interconnecting said processing nodes through a multi-stage communication network;

Cancelled

computer readable program code means for causing a computer to effect storing at each said processing node a plurality of cache lines in one or more caches;

computer readable program code means for causing a computer to effect tracking in a cache coherency directory which is distributed to each of said processing nodes which of said processing nodes have copies of each cache line; and

computer readable program code means for storing changed data immediately to said unique section of shared memory regardless of which of said nodes is changing the data and which of said nodes includes the section of shared memory to be changed such that said shared memory always contains the most recent data.

34. [Amended] A computer program product or computer program element for operating a shared memory parallel processing system including a plurality of processing nodes, each said node including a unique section of shared memory which is not a cache, according to the steps of:

Rejected

interconnecting said processing nodes through a multi-stage communication network;

storing at each said processing node a plurality of cache lines in one or more caches;

distributing to each of said processing nodes a cache coherency directory;

tracking in said cache coherency directory which of said processing nodes have copies of each cache line; and

storing changed data immediately to said unique section of shared memory regardless of which of said nodes is changing the data and which of said nodes includes the

section of shared memory to be changed such that said shared memory always contains the most recent data.

37. [Amended] The cache coherency system of claim 36, further comprising at a first node of said plurality of processing nodes a memory controller selectively operable first responsive to a request for access to a memory word by first accessing the cache at said first node and, if said requested memory word is not available in said cache, selectively operable second for accessing said memory word selectively from said shared memory regardless of which of said nodes includes the section of shared memory being accessed, and storing said cache line including said memory word to said cache at said first node.

38. [Amended] The cache coherency system of claim 37, said memory controller further being selectively operable for deleting a cache line from said cache at said first node when said cache is full to provide space for a new cache line to be stored to said cache, and for sending the address of the deleted cache line to an invalidation directory to indicate said node no longer has a copy of said cache line.